Basic Wafer Definitions

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The article is a quick and simple reference to many basic wafer definitions. For a complete, and very detailed listing of wafer definitions one is advised to review the published SEMI Specifications for Silicon Wafers (SEMI), or other more detailed articles in the VSI Technology Library.

Conductivity Type: Defines the type of charged-carrier in the crystal that is conducting electricity.

- ***n-type*** – Si material having electrons as the majority current carriers. Electrons have negative charge (n). Doping with the impurities Phosphorous, Antimony and Arsenic creates n-type material.
- ***p-type*** - Si material having holes as the majority current carriers. Holes have positive charge (p). Doping with the impurity Boron creates p-type material.

Resistivity: The resistance to current flow and movement of electron and hole carries in the silicon. Resistivity is related to the ratio of voltage across the silicon to the current flowing through the silicon per unit volume of silicon. The units for resistivity are *Ohm-cm*, and these are the units used to specify the resistivity of silicon wafers and crystals. Resistivity is controlled by adding impurities such as As, Phos., and Boron to the silicon. As the amount of impurity or dopant is increased, the resistivity is decreased. Heavy doped material has low resistivity.

Dopant: An intentional impurity such as As, Phos., or Boron added to the silicon to engineer or alter the resistivity. As the dopant increases in concentration per cubic cm the resistivity is reduced. Typical dopant levels in silicon are 1-100 ppma.

Sheet Resistance: The resistance to current flow and movement of electron and hole carries in the silicon. Sheet resistance is related to the ratio of voltage across the silicon to the current flowing through the silicon per unit surface area of silicon. The units for Sheet Resistance are *Ohm/Square*, and these are the units typically used to specify the sheet resistance of silicon wafers having an epitaxial or diffusion layer on the surface.

Diameter: The normal width across the wafer or diameter of the silicon wafer not in the region of the flats or other marks. Typical and standard silicon wafer diameters are: 25.4mm (1”), 50.4mm (2”), 76.2mm (3”), 100mm, 125mm, 150mm, 200mm, 300mm.

Thickness: The normal distance through a slice or wafer in a direction normal to the surface at a given point.

Total Thickness Variation (TTV): The maximum variation in the wafer thickness. Total Thickness Variation is generally determined by measuring the wafer in 5 locations of a cross pattern (not too close to the wafer edge) and calculating the maximum measured difference in thickness.

Orientation: The growth plane of the crystalline silicon. Orientations are described using Miller Indices such as (100), (111), (110), (211), etc. Different growth planes and orientations have different arrangements of the atoms or lattice as viewed from a particular angle.

Slice Orientation: The crystallographic orientation of the surface of a wafer. The primary and most common slice orientations are (100), (111) and (110).

Primary Flat: The flat of longest length appearing in the circumference of the wafer. The primary flat has a specific crystallographic orientation relative to the wafer surface.

Secondary Flat: The flat of shortest length appearing in the circumference of the wafer. The primary flat has a specific crystallographic orientation relative to the wafer surface and the primary flat.

Bow: Concavity, curvature, or deformation of the wafer centerline independent of any thickness variation present.

Warp: Deviation from a plane of a slice or wafer centerline containing both concave and convex regions.

Haze Free: A silicon wafer having the best possible surface finish and micro-roughness on the order of less than 10A.

Prime Grade: The highest grade of a silicon wafer. SEMI indicates the bulk, surface, and physical properties required to label silicon wafers as “Prime Wafers”.

Reclaim Grade: A lower quality wafer that has been used in manufacturing and then reclaimed , etched or polished, and then used a second time in manufacturing.

Test Grade: A virgin silicon wafer of lower quality than Prime, and used primarily for testing processes. SEMI indicates the bulk, surface, and physical properties required to label silicon wafers as “Test Wafers”.

SOI: Silicon-on-Insulator (SOI) wafers are silicon wafers having an oxide layer buried below the surface of the crystalline silicon. The wafer is a stack of material with silicon on top of oxide on top of silicon. SOI wafers can be created by: 1) bonding two oxidized

piece of silicon together (bonded wafers) to form the stack, or 2) by using a heavy oxygen ion implant of the wafer followed by annealing (often known as SIMOX).