Technical Note on VSI UltraThin® SOI and Thin-Wafer-Bonding US Patent

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A Background on Intellectual Property and Technology

Over the past 10 years, VSI has demonstrated direct or fusion bonding of thin-silicon device-wafers to thicker handle-wafers where the device wafer ranges in thickness from 25um to 200um. This UltraThin® SOI technology allows the direct bonding of patterned device wafers or simple, bare, silicon layers to a handle wafer without the need for subsequent grinding and polishing of the device layer.

VSI owns all rights and intellectual property related to the bonding of silicon wafers less than 200um thick to a second silicon wafer as described in US Patent 5,843,832 [1]. The claims in this US Patent cover all techniques, equipment, and fixtures typically used to manufacture bonded silicon wafers.

The IP defined by US Patent 5,843,832 includes the bonding of bare silicon wafers for applications in electronic devices such as Microwave PIN diodes, as well as wafers including a silicon-dioxide layer for applications requiring silicon-on-insulator (SOI) substrates.

The invention describes a bonding system for ULTRATHIN® wafers [2] and a bonded wafer product that has two joined materials, one of which is thinner than 200um. More specifically, the present invention defines a technique which can be used to form a bonded product including at least one ULTRATHIN® wafer, having improved characteristics for optical, electrical, and mechanical applications.

ULTRATHIN® wafers have been bonded to a handle substrate using direct or fusion bonding. The fusion bonding typically uses a heat process to fuse the silicon wafers to one another or to an oxide layer there between. This technique brings the thin wafer into contact with a substrate, and then the two are annealed together at an elevated temperature to promote adhesion. Anodic bonding requires that the thin wafer be brought in contact with the handle wafer, and then adhesion is promoted by applying an electrical bias. Annealing may follow the anodic bonding process.

VSI uses proprietary and unique wafer processing procedures to fabricate ULTRATHIN® wafers having low total thickness variation and extremely low micro-roughness that is required for successful direct bonding of silicon wafers. Void free and high performance SOI and Si-Si wafers have been fabricated using thin wafer bonding.

Figure 1 is taken directly from the US Patent and identifies the overall bonding process.

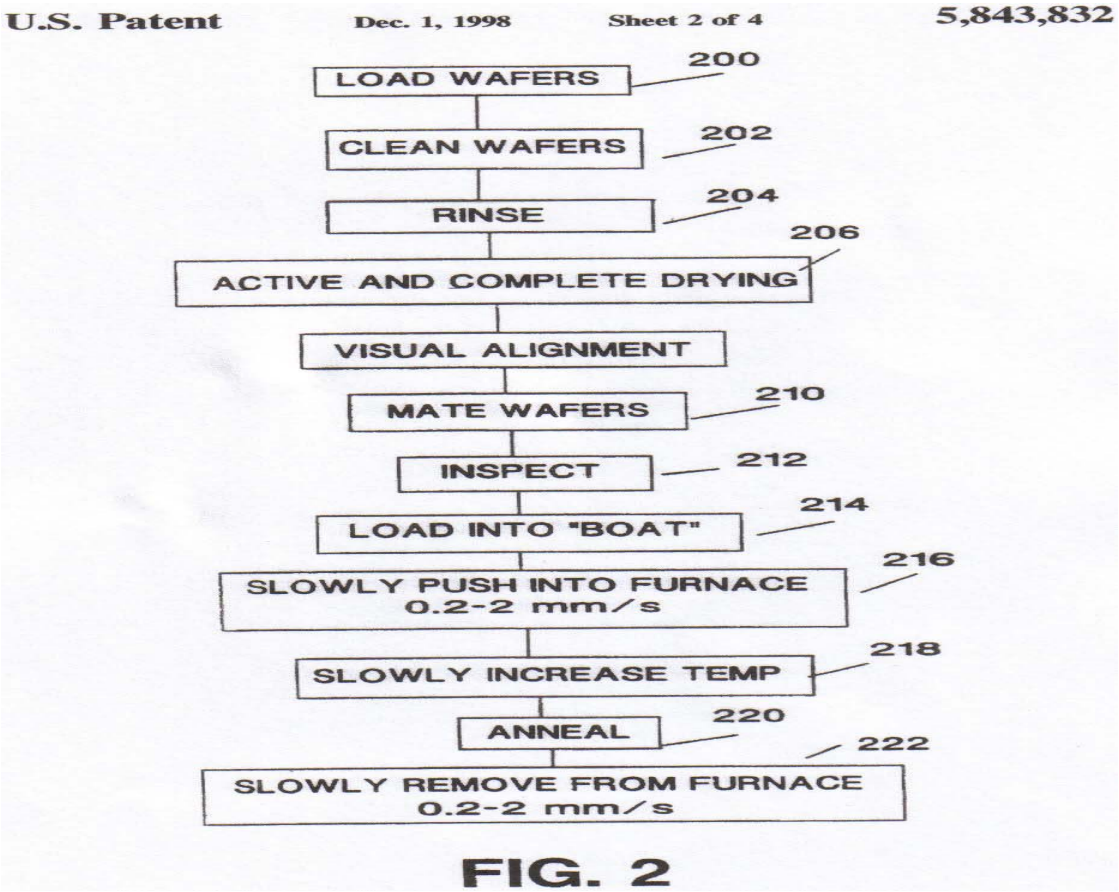
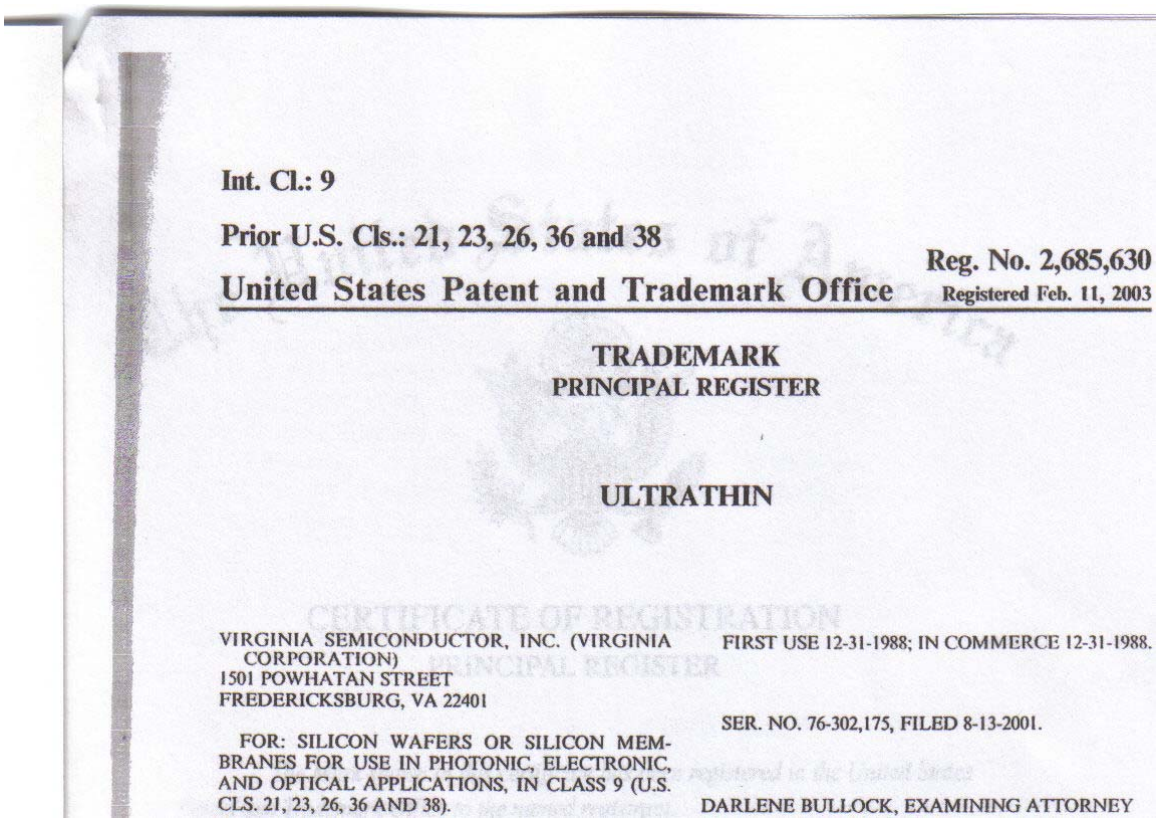


Figure 1 General Technique for wafer Bonding

VSI has manufactured and sold ULTRATHIN® silicon wafers less than 200um for over 10 years (<100> orientation wafers ranging in thickness from 8um-200um). These wafers have the needed low micro-roughness and flatness for successful bonding to handle wafers. VSI owns all rights to the US Trademark ULTRATHIN® as related to thin silicon wafers.

Figure 2 is a copy of the US Trademark registration on ULTRATHIN® .



Int. Cl.: 9

Prior U.S. Cls.: 21, 23, 26, 36 and 38

United States Patent and Trademark Office

Reg. No. 2,685,630

Registered Feb. 11, 2003

TRADEMARK
PRINCIPAL REGISTER

ULTRATHIN

VIRGINIA SEMICONDUCTOR, INC. (VIRGINIA CORPORATION)
1501 POWHATAN STREET
FREDERICKSBURG, VA 22401

FOR: SILICON WAFERS OR SILICON MEMBRANES FOR USE IN PHOTONIC, ELECTRONIC, AND OPTICAL APPLICATIONS, IN CLASS 9 (U.S. CLS. 21, 23, 26, 36 AND 38).

FIRST USE 12-31-1988; IN COMMERCE 12-31-1988.

SER. NO. 76-302,175, FILED 8-13-2001.

DARLENE BULLOCK, EXAMINING ATTORNEY

Figure 2 VSI, US Trademark on the use of ULTRATHIN

B Claims Related to Bonding Silicon <200um thin

Figure 3,4 are taken from the US Patent and clearly articulate intellectual property ownership for bonding silicon wafers <200um thin using any known methods, techniques, fixtures, and equipment.

What is claimed is:

1. A method of bonding a thin wafer having a thickness less than 200 μm to another wafer, comprising:

washing said thin wafer and said another wafer;

completely drying said wafers;

aligning said wafers in a definite crystallographic orientation relative to one another;

loading said wafers into a device with a divider between said thin wafer and said another wafer;

slowly removing said wafers from said device, so that a first portion of said wafers comes into contact, while said divider separates other portions of said wafers against coming into contact;

continuing to remove said wafers until said wafers are completely in contact with one another to bond said wafers to one another; and

increasing a strength of the bond of said contacted wafers.

2. A method as in claim 1, wherein said increasing step comprises annealing said wafers.

3. A method as in claim 2, wherein said annealing comprises:

loading said bonded wafers into a receptacle;

inserting said receptacle into a heating oven to gradually heat said bonded wafers at an insertion rate sufficiently slow to maintain substantial isothermy throughout said wafers; and

curing said wafers in said heated oven.

4. A method as in claim 3, wherein said annealing further comprises cooling said wafers at a rate sufficiently slow to maintain substantial isotherms throughout said wafers.

5. A method as in claim 3, wherein said insertion rate of said receptacle is substantially 0.5 mm/s.

6. A method as in claim 4, wherein said cooling step includes removing said receptacle from said heating oven at a speed of substantially 0.5 mm/s.

7. A method as in claim 1, wherein said removing step comprises removing said wafers at a rate slower than the propagation speed of a contact wave which would result in the absence of a spacer.

8. A method as in claim 1, wherein said completely drying step comprises blow drying said wafers with an inert gas.

9. A method as in claim 1, wherein said washing washes said wafers while said wafers are loaded in said device.

10. A method of bonding a first thin wafer having a thickness which is less than 200 μm, to another second wafer, comprising:

loading said first and second wafers into a wafer holding device which has a divider between said first and second wafers;

washing said first and second wafers;

completely drying said wafers;

aligning said wafers in a definite crystallographic orientation relative to one another;

contacting said wafers to one another;

bonding said wafers by removing said wafers from said device,

such that during the removing step, at least a first portion of said wafers comes into mutual contact while other portions of said wafers are held apart by said divider, and after the removing step no part of said wafers are held apart by said divider;

heating said contacted wafers, by gradually increasing a temperature thereof until reaching a bonding temperature to strengthen a bond of said contacted wafers to one another, said heating being sufficiently slow to maintain substantial isothermy in said wafers; and

gradually decreasing a temperature of said contacted wafers after bonding.

11. A method as in claim 10, further comprising annealing said wafers during said bonding.

12. A method as in claim 11, wherein said heating comprises:

loading said contacted wafers into a receptacle;

inserting said receptacle into a heated oven to gradually heat said contacted wafers at substantially 0.5 mm/s; and

curing said wafers in said heated oven.

13. A method as in claim 10, wherein said contacting comprises:

slowing removing said wafers from said device, at a rate slower than the propagation speed of a contact wave formed by said mutual contact, so that a first portion of said wafers comes into contact, while said divider separates other portions of said wafers against coming into contact; and

continuing to remove said wafers until said wafers are completely in contact with one another.

14. A method as in claim 10, wherein said completely drying step comprises blow drying said wafers in inert gas.

15. A method of bonding an ultra-thin silicon wafer to a semiconductor substrate, comprising:

obtaining an ultra-thin wafer, having a thickness which is less than 200 μm;

bringing the ultra-thin wafer towards a wafer to which said ultrathin wafer will be bonded, by:

a) maintaining a separation between said substrates at a time prior to bonding,

b) aligning said wafers in a definite crystallographic orientation prior to bonding; and

c) mutually contacting said wafers in said predetermined crystallographic orientation, such that said wafers contact each other in a manner sufficiently slowly so that a first portion of said wafers comes into contact and the speed at which succeeding portions of the wafers come into contact is less than a propagation speed of a contact wave which would result in the absence of a spacer; and

d) subsequent to said wafers touching, further bonding said wafers to one another using an annealing process.

16. A method as in claim 15 wherein said maintaining comprises using a divider to divide said wafers from one another.

17. A method of bonding an ultra-thin wafer having a thickness less than 200 μm to a semiconductor substrate, comprising:

obtaining a semiconductor substrate;

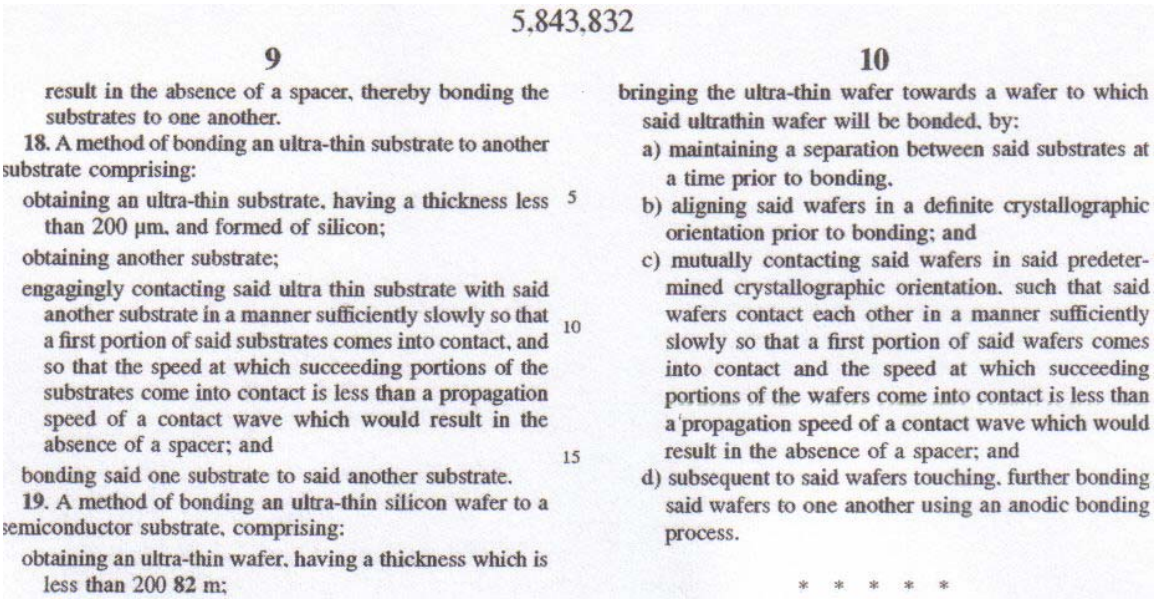
obtaining an ultra-thin wafer of silicon having a thickness less than 200 μm;

crystallographically aligning said ultra thin wafer and said substrate;

separating the substrates while the substrates are aligned and maintaining their alignment; and

allowing the substrates to touch one another, such that said substrates contact each other in a manner sufficiently slowly so that a first portion of said wafers comes into contact, and the speed at which succeeding portions of the wafers come into contact is less than a propagation speed of a contact wave which would

Figure 3 Bonded Wafer Claims 1-17



5,843,832

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result in the absence of a spacer, thereby bonding the substrates to one another.

18. A method of bonding an ultra-thin substrate to another substrate comprising:

obtaining an ultra-thin substrate, having a thickness less than 200 μm, and formed of silicon;

obtaining another substrate;

engagingly contacting said ultra thin substrate with said another substrate in a manner sufficiently slowly so that a first portion of said substrates comes into contact, and so that the speed at which succeeding portions of the substrates come into contact is less than a propagation speed of a contact wave which would result in the absence of a spacer; and

bonding said one substrate to said another substrate.

19. A method of bonding an ultra-thin silicon wafer to a semiconductor substrate, comprising:

obtaining an ultra-thin wafer, having a thickness which is less than 200 82 m;

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bringing the ultra-thin wafer towards a wafer to which said ultrathin wafer will be bonded, by:

a) maintaining a separation between said substrates at a time prior to bonding,

b) aligning said wafers in a definite crystallographic orientation prior to bonding; and

c) mutually contacting said wafers in said predetermined crystallographic orientation, such that said wafers contact each other in a manner sufficiently slowly so that a first portion of said wafers comes into contact and the speed at which succeeding portions of the wafers come into contact is less than a propagation speed of a contact wave which would result in the absence of a spacer; and

d) subsequent to said wafers touching, further bonding said wafers to one another using an anodic bonding process.

* * * * *

Figure 4 Bonded Wafer Claims 18,19

The reader is recommend to review US Patent 5,843,832 in full detail as needed, and this article only serves as a technical note and overview.

IP Licensing

If technical access to this IP is needed, contact VSI immediately for detailed discussion of IP licensing. Virginia Semiconductor is interested in the advancement of the technology described in this article.

C References

[1] US Patent 5,843,832, Assignee Virginia Semiconductor Incorporated, Inventors K. R. Farmer, T.G. Digges, Jr., N.P. Cook, issued December 1, 1998.

[2] US Trademark 2,685,630, ULTRATHIN®, Virginia Semiconductor Incorporated, Registered February 11, 2003.